UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,629	03/03/2004	Soo-Chan Lee	2421-000033/US	3096

7590 06/06/2007

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER
HOLLINGTON, JERMELE M

ART UNIT	PAPER NUMBER
2829	

MAIL DATE	DELIVERY MODE
06/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/791,629	LEE ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34 and 37-42* is/are pending in the application.

4a) Of the above claim(s) *11-32,38 and 39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 33-34, 37 and 40-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10, 33-34, 37 and 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Shim et al (6844717).

Regarding claim 1, Shim et al disclose [see Figs. 1-3] a semiconductor device test apparatus comprising a main body (main body 1) including a sorting robot (combination of tray arrangement stations 80-82) disposed thereon to move along an X-axis, and a loading robot (loading robot 90) and an unloading robot (unloading robot 91 and 92) disposed thereon to each move along both an X-axis and Y-axis; a soak chamber (soak chamber 50), a test chamber (test heads 100 and 101); a desoak chamber (desoak chamber 60); wherein the soak chamber (50), the test chamber (100 and 101), and the desoak chamber (60) are attached to the main body (1) and separable from the main body (1).

Regarding claim 2, Shim et al disclose the soak chamber (50), the test chamber (100 and 101), and the desoak chamber (60) are separable from the main body (1) using a sliding unit.

Regarding claim 3, Shim et al disclose a semiconductor device test apparatus comprising: a main body (main body 1) including a sorting robot (combination of tray arrangement stations

80-82) disposed thereon to move along an X-axis, and a loading robot (loading robot 90) and an unloading robot (unloading robot 91 and 92) disposed thereon to each move along both an X-axis and Y-axis; and a stacker (combination of tray supplier 10 and tray deliverer 20) for stacking devices (ICs) before and after a test, the stacker (10 and 20) including user trays (test trays 70) for stacking the devices (ICs), wherein the user trays (70) are interchangeable such that the user trays (70) may be being used to stack the devices (ICs) prior to the test and to stack the devices (ICs) after the test.

Regarding claim 4, Shim et al disclose the user trays (70) are interchangeable in accordance with the process of the test.

Regarding claim 5, Shim et al disclose a semiconductor device test apparatus comprising: a main body (main body 1) including a sorting robot (combination of tray arrangement stations 80-82) disposed thereon to move along an X-axis, and a loading robot (loading robot 90) and an unloading robot (unloading robot 91 and 92) disposed thereon to each move along both an X-axis and Y-axis; a stacker (10 and 20) for stacking devices (ICs) before and after a test, the stacker (10 and 20) including at least one user tray feeder (tray supplier 10) predesignated with a function for stacking un-tested devices (ICs) and at least one user tray sender (tray deliverer 20) predesignated with a function, for stacking tested devices (ICs), wherein the user tray (70) functions being interchangeable during stacker operation.

Regarding claim 6, Shim et al disclose a semiconductor device test apparatus comprising: a main body (main body 1) including a sorting robot (combination of tray arrangement stations 80-82) disposed thereon to move along an X-axis, and a loading robot (loading robot 90) and an unloading robot (unloading robot 91 and 92) disposed thereon to each move along both an X-

axis and Y-axis; and a stacker (10 and 20) arranged in the main body (1), the stacker (10 and 20) having a user tray feeder (10) which loads a plurality of user trays (70) having a desired quantity of devices (ICs) to be tested and a user tray sender (20) which loads the plurality of user trays (70) having the devices sorted by their grades in accordance with the test result, the user tray feeder (10) and the user tray sender (20) interchangeable in their uses in accordance with the process of the test.

Regarding claim 7, Shim et al disclose a soak chamber (50) for receiving the test tray (70) inputted from the device loader (loader side plate 30), and for preheating or precooling the devices (ICs); a test chamber (100 and 101) for connecting the preheated devices (ICs) in the soak chamber (50) to a socket of a test head (100) and for performing a test; a desoak chamber (60) for receiving the test tray (70) discharged from the test chamber (100 and 101) and for discharging them to a device unloader (unloader side plate 40) after recovering them to a room temperature, wherein the soak chamber (50), the test chamber (100 and 101) and the desoak chamber (60) are separable from the main body (1) using a sliding unit.

Regarding claim 8, Shim et al disclose the soak chamber (50) and the test chamber (100 and 101) are made of one body to be separated in the same direction.

Regarding claim 9, Shim et al disclose the desoak chamber (60) is separated in same direction as the separation direction of the soak chamber (50) and the test chamber (100 and 101).

Regarding claim 10, Shim et al disclose a loading robot (90) for picking up devices (ICs) to be tested, which are in a stand-by status in the user tray feeder (10) and mounting them on a test tray (70) being on a device loading stage (30); a sorting robot (80) for picking up the device

discharged to the device unloader (40) and for carrying them to a plurality of sorter tables in accordance with the test result; and an unloading robot (91 and 92) for picking up the device carried to the sorter table and for carrying them to the user tray sender (20).

Regarding claim 33, Shim et al disclose a semiconductor device test apparatus comprising a loading robot (90) to move along a X-axis and a Y-axis for picking up devices (ICs) to be tested, which are in a stand-by status in the user tray feeder (10) and mounting them on a test tray (70) being on a device loading stage (30); a sorting robot (80) to move along a X-axis for picking up the device discharged to the device unloader (40) and for carrying them to a plurality of sorter tables in accordance with the test result; and an unloading robot (91 and 92) for picking up the device carried to the sorter table and for carrying them to the user tray sender (20), and the unloading robot (91 and 92) to move along an X-axis and Y-axis, wherein the operating speed of the loading robot (90), the sorting robot (80) and the unloading robot (91 and 92) is determined based on the speed of testing the device (ICs).

Regarding claim 34, Shim et al disclose a robot including a sorting robot (combination of tray arrangement stations 80-82) disposed thereon to move along an X-axis, and a loading robot (loading robot 90) and an unloading robot (unloading robot 91 and 92) disposed thereon to each move along both an X-axis and Y-axis used in a test that receives control signals instructing the robot to carry a device (ICs) at a calculated speed, the calculated speed corresponding based on a time of test execution.

Regarding claim 37, Shim et al disclose a method for stacking devices (ICs) in a semiconductor test apparatus comprising, predesignating at least one user tray feeder (10) for stacking un-tested devices, predesignating at least one user tray sender (20) for stacking tested

devices, designating at least one user tray feeder (10) for stacking tested devices based on the test; stacking at least one tested device (ICs) on the at least one user tray feeder (10).

Regarding claim 40, Shim et al disclose a method for controlling a robot speed of a semiconductor device test apparatus, comprising the steps of: sending control signals to at least one robot (90) to carry a device (ICs) for a test detecting a time for the test; calculating a desired speed value of the robot (90) corresponding to the test time detected, and informing the corresponding robot (90) of the calculated speed value to control the speed of the robot (90).

Regarding claim 41, Shim et al disclose the time for the test begins when the device (ICs) contacts a test head (tester head 100 and 101) and ends when the device (ICs) is released from the socket.

Regarding claim 42, Shim et al disclose the step of detecting the time for the test includes retrieving stored values of pretested, like kind devices.

Conclusion

3. Applicant's arguments with respect to claims 1-10, 33-34, 37 and 40-42 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:00 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
May 31, 2007